LISTING OF THE CLAIMS:

The following is a complete listing of all the claims in the application, with an indication of the status of each.

1. (Currently Amended) A data processing device including:

    a processor;

    a charge storage device coupled to the processor;

    a current source for supplying the processor with substantially constant operating current at <u>a level switchable among</u> multiple nonzero current levels, and adapted to <u>switch the level of the</u> ~~vary its~~ output <u>operating</u> current independently of an instantaneous power demand of the processor by switching<u>,</u> <u>on at least one of a periodic and an aperiodic basis, among</u> ~~either periodically or~~ ~~aperiodically between~~ the multiple nonzero current levels.

2. (Currently Amended) The device of claim 1 <u>wherein</u> ~~in which~~ the charge storage device comprises a capacitor in series with the current source, and across which the processor is connected in parallel.

3. (Currently Amended) The device of claim 1 <u>wherein</u> ~~in which~~ the current source is adapted to ~~periodically or aperiodically~~ switch between two different nonzero current levels.

4. (Canceled)

1 5. (Currently Amended) The device of claim 3 wherein in which the current

2 source is adapted to determine the interval between switching current levels

3 based on is determined by an average power demand of the processor.

1 6. (Currently Amended) The device of claim 1 wherein in which the current

2 source further comprises:

3   a second current source adapted to provide a noise current, superposed on

4 the substantially constant current, that varies on at least one from among a

5 random and or pseudo-random basis.

1 7. (Currently Amended) The device of claim 1 further including a control means

2 for controlling the current source adapted to maintain the supply voltage to the

3 processor between an upper voltage limit and a lower voltage limit.

1 8. (Currently Amended) The device of claim 1 further including a zener diode

2 connected to the processor adapted to maintain the supply voltage to the

3 processor between an upper voltage limit and a lower voltage limit.

1 9. (Currently Amended) The device of claim 7 wherein in which the control

2 means includes a current switching means for switching the current source

3 between a first, higher current level and a second, lower current level, the

4 current level switching being triggered by the supply voltage to the processor

5 respectively reaching the lower voltage limit and the upper voltage limit.

10. (Original) The device of claim 9 further including a timer for determining a time period taken for the processor supply voltage to reach a lower voltage limit from an upper voltage limit, or vice versa.

11. (Currently Amended) The device of claim 10 <u>wherein the timer determines whether the time period falls outside predetermined limits, and</u> further including current setting means for varying <u>at least one from among</u> the first current level <u>and</u> ~~and/or~~ the second current level of the current source if the timer determines that the time period falls outside <u>the</u> predetermined limits.

12. (Currently Amended) The device of claim 11 <u>wherein the predetermined limits include a first predetermined threshold, and wherein</u> ~~in which~~ the current setting means raises the first current level if the timer determines that the time period for reaching the lower voltage limit falls below <u>the</u> [[a]] first predetermined threshold.

13. (Currently Amended) The device of claim 11 <u>wherein the predetermined limits include a second predetermined threshold, and wherein</u> ~~in which~~ the current setting means reduces the first current level if the timer determines that the time period for reaching the lower voltage limit exceeds <u>the</u> [[a]] second predetermined level.

1   14. (Currently Amended) The device of claim 11 <u>wherein the predetermined</u>

2   <u>limits include a first predetermined threshold, and wherein</u> <s>in which</s> the

3   current setting means reduces the second current level if the timer determines

4   that the time period for reaching the upper voltage limit exceeds <u>the</u> [[a]] first

5   predetermined level.

1   15. (Currently Amended) The device of claim 11 <u>wherein the predetermined</u>

2   <u>limits include a second predetermined threshold, and wherein</u> <s>in which</s> the

3   current setting means raises the second current level if the timer determines

4   that the time period for reaching the upper voltage limit exceeds <u>the</u> [[a]] second

5   predetermined level.

1   16. (Currently Amended) The device of claim 9 <u>wherein</u> <s>in which</s> the control

2   means includes means for temporarily inhibiting the current switching means if

3   the supply voltage to the processor fails to move towards the <s>desired</s> upper

4   <u>voltage limit</u> or <u>the</u> lower voltage limit.

1   17. (Currently Amended) The device of claim 1 <u>wherein</u> <s>in which</s> the processor

2   has an internal clock <u>having a</u> <s>,the</s> frequency <u>that</u> <s>of which</s> is dependent upon

3   the supply voltage to the processor.

1   18. (Currently Amended) The device of claim 1 <u>wherein</u> <s>in which</s> the processor

2   is a cryptographic processor.

1   19. (Currently Amended) The device of claim 1 <u>further comprising a</u>

2   ~~incorporated into~~ a smart card <u>supporting the processor, the charge storage</u>

3   <u>device, and the current source</u>.

1   20. (Currently Amended) A method of operating a data processing device <u>having</u>

2   <u>a processor and a charge storage device connected to the processor</u>, comprising

3   ~~the steps of~~:

4   drawing <u>a substantially constant</u> current from an external power supply

5   <u>at a level switchable among multiple nonzero levels</u>; <u>and</u>

6   ~~utilizing the drawn current to~~ cyclically apportion<u>ing the</u> [[a]]

7   substantially constant current flow from <u>the</u> current source between a charge

8   storage device and <u>the</u> [[a]] processor ~~within the data processing device~~,

9   <u>wherein the step of cyclically apportioning the substantially constant</u>

10 <u>current flow switches the drawn current level</u> ~~that is periodically or~~

11 ~~aperiodically switched~~ between <u>the</u> multiple different nonzero <u>substantially</u>

12 <u>constant</u> current levels <u>at one from among a periodic and aperiodic basis, the</u>

13 <u>switching being</u> such that the drawn current varies independently of the

14 instantaneous power demand of the processor.

1   21. (Currently Amended) The method of claim 20 <u>wherein</u> ~~further including~~ the

2   step of ~~utilizing the drawn current to generate~~ <u>cyclically apportioning</u> a current

3   flow to the processor and the charge storage device <u>switches the level of the</u>

4   drawn current, ~~that is~~ periodically or aperiodically, ~~switched~~ between two

5   different nonzero substantially constant current levels.

22. (Cancelled)

1   23. (Currently Amended) The method of claim 21 wherein ~~further including~~ the

2   step of cyclically apportioning a current flow includes determining the interval

3   between switching according to an average power demand of the processor.

1   24. (Currently Amended) The method of claim 20 wherein the step of cyclically

2   apportioning a substantially constant current flow utilizes a first current

3   source, and further including ~~the steps of~~:

4   utilizing a second current source to provide a superposed current that

5   varies on a random or pseudorandom basis and

6   delivering the combined current of the first and second current sources to

7   the processor and the charge storage device.

1   25. (Previously Presented) The method of any one of the claims 20, 21, 23, and

2   24 further including the step of maintaining a supply voltage to the processor

3   between an upper voltage limit and a lower voltage limit.

1   26. (Currently Amended) The method of claim 25 wherein ~~further including~~ the

2   step of cyclically apportioning a substantially constant current flow switches the

3   ~~switching a~~ current level ~~source~~ between a first, higher current level and a

4   second, lower, current level, when the supply voltage to the processor

5   respectively reaches the lower voltage limit and the higher voltage limit.

1   27. (Currently Amended) The method of claim 26 <u>wherein the step of cyclically</u>

2   <u>apportioning a substantially constant current flow</u> further <u>includes</u> ~~including~~

3   the steps of:

4   determining a time period taken for the processor supply voltage to reach

5   a lower voltage limit from an upper voltage limit, or vice versa, and

6   varying the first current level and/or the second current level of the

7   current ~~source~~ if the time period falls outside predetermined limits.

1   28. (Currently Amended) The method of claim 27 <u>wherein said step of varying</u>

2   further <u>includes</u> ~~including the step of~~ raising the first current level if the time

3   period for reaching the lower voltage limit falls below a first predetermined

4   threshold.

1   29. (Currently Amended) The method of claim 27 <u>wherein said step of varying</u>

2   further <u>includes</u> ~~including the step of~~ reducing the first current level if the time

3   period for reaching the lower voltage limit exceeds a second predetermined

4   threshold.

1   30. (Currently Amended) The method of claim 27 <u>wherein said step of varying</u>

2   further <u>includes</u> ~~including the step of~~ reducing the second current level of the

3   time period for reaching the upper voltage limit falls below a first

4   predetermined threshold.

1   31. (Currently Amended) The method of claim 27 <u>wherein said step of varying</u>

2   further <u>includes</u> ~~including the step of~~ raising the second current level if the time

3   period for reaching the upper voltage limit exceeds a second predetermined

4   threshold.

1   32. (Currently Amended) The method of claim 26 further including the step of

2   temporarily inhibiting the current switching if the supply voltage to the

3   processor fails to move towards the ~~desired~~ upper <u>voltage limit</u> or <u>the</u> lower

4   voltage limit.

1   33. (Original) The method of claim 20 further including the step of controlling

2   the frequency of operation of the processor as a function of the supply voltage to

3   the processor.

34-35. (Canceled)

1   36. (Currently Amended) The method of claim 28 <u>wherein said step of varying</u>

2   further <u>includes</u> ~~including the step of~~ reducing the first current level if the time

3   period for reaching the lower voltage limit exceeds a second predetermined

4   threshold.